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                      MULTIPLE CACHE CONFIGURATIONS

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## METHOD AND SYSTEM FOR SUPPORTING MULTIPLE CACHE CONFIGURATIONS

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### BACKGROUND OF THE INVENTION

Referring to **FIG. 1**, an electrical coupling network between a static random access memory **20a** (hereinafter “SRAM **20a**”) and a static random access memory **20b** (hereinafter “SRAM **20b**”) is shown. SRAM **20a** and SRAM **20b** are identical memory devices. Specifically, both SRAM **20a** and SRAM **20b** have an identical pin arrangement including seven (7) rows and seventeen (17) columns of pins. The first column of pins are shown in **FIG. 1**. In the first column of pins, SRAM **20a** includes two (2) output power supply pins **21a** and **27a**, and  
10 SRAM **20b** includes two (2) output power supply pins **21b** and **27b**. Also in the first column of pins, SRAM **20a** includes four (4) synchronous address input pins **22a**, **23a**, **25a**, and **26a**, and SRAM **20b** includes four (4) synchronous address input pins **22b**, **23b**, **25b**, and **26b**. Pin **24a** of SRAM **20a** and pin **24b** of SRAM **20b** are not utilized.

20 In support of four (4) cache configurations, SRAM **20a** is mounted to a front side of a processor card **10**, and SRAM **20b** is mounted to a rear side of processor card **10**. SRAM **20a** and SRAM **20b** are positioned with an alignment of pin **21a** and pin **27b**, an alignment of pin **22a** and pin **26b**, an alignment of pin **23a** and pin **25b**, an alignment of pin **24a** and pin **24b**, an alignment of pin **25a** and pin **23b**, an alignment of pin **26a** and pin **22b**, and an alignment of pin **27a**  
25 and pin **21b**.

Pin **22a** and pin **22b** are functionally equivalent and electrically coupled via a conductor **28a** within processor card **10** to concurrently receive a first address bit signal from a microprocessor. Pin **23a** and pin **23b** are functionally equivalent and electrically coupled via a conductor **28b** within processor card **10** to concurrently receive a second address bit signal from the microprocessor. Pin **25a** and pin **25b** are functionally equivalent and electrically coupled via a conductor **28c** within processor card **10** to concurrently receive a third address bit signal from the microprocessor. Pin **26a** and pin **26b** are functionally equivalent and electrically coupled via a conductor **28d** within processor card **10** to concurrently receive a fourth address bit signal from the microprocessor. The four (4) address bits signal are selectively provided by the microprocessor as a function of a selected cache configuration.

A drawback associated with the aforementioned electrical couplings as shown is the length of conductors **28a–28d** tends to establish a maximum frequency at which the microprocessor can effectively and efficiently control SRAM **20a** and SRAM **20b**, and the established maximum frequency can be significantly lower than a desired operating frequency of the microprocessor. The computer industry is therefore continually striving to improve upon the electrical coupling between the synchronous address input pins of SRAM **20a** and SRAM **20b** whereby a maximum frequency at which a microprocessor can effectively and efficiently control SRAM **20a** and SRAM **20b** matches a desired operating frequency of the microprocessor. The computer industry is also continually striving to improve upon the electrical communication of a selected cache configuration from a microprocessor to the synchronous address input pins of SRAM **20a** and SRAM **20b**.

Field Of The Invention

The present invention generally relates to computer hardware mounted upon a processor card, and in particular to an electrical coupling between  
5 memory components for supporting multiple cache configurations and an electrical communication from a microprocessor to the memory components for selecting one of the supported multiple cache configurations.

SUMMARY OF THE INVENTION

10 One form of the present invention is a processor card having a first memory device and a second memory device mounted thereon. The first memory device includes a first address pin and a second address pin. The second memory device includes a third address pin and a fourth address pin. The first address pin of the first memory device and the third address pin of the  
15 second memory device are functionally equivalent address pins. The second address pin of the first memory device and the fourth address pin are functionally equivalent address pins. The first address pin of the first memory device and the fourth address pin of the second memory device are electrically coupled to thereby concurrently receive a first address bit signal. The second address pin of  
20 the first memory device and the third address pin of the second memory device are electrically coupled to thereby concurrently receive a second address bit signal.

Another form of the present invention is a system including a first memory device, a second memory device, and a microprocessor. The first memory  
25 device includes a first address pin and a second address pin. The second memory device includes a third address pin and a fourth address pin. The first address pin of the first memory device and the third address pin of the second memory device are functionally equivalent address pins. The second address pin of the first memory device and the fourth address pin are functionally

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equivalent address pins. The microprocessor is operable to concurrently provide a first address bit signal to first address pin of the first memory device and the fourth address pin of the second memory device. The microprocessor is further  
5 operable to concurrently provide a first address bit signal to second address pin of the first memory device and the third address pin of the second memory device.

The foregoing and other features and advantages of the invention will become further apparent from the following detailed description of the presently  
10 preferred embodiments, read in conjunction with the accompanying drawings. The detailed description and drawings are merely illustrative of the invention rather than limiting, the scope of the invention being defined by the appended claims and equivalents thereof.

15 BRIEF DESCRIPTION OF THE DRAWINGS

**FIG. 1** is a fragmented side view of a processor card having a pair of static random accesses memories mounted thereon with an electrical coupling of synchronous address pins as known in the art;

**FIG. 2** is view of the **FIG. 1** processor card and **FIG. 1** static random  
20 accesses memories with an electrical coupling of synchronous address pins in accordance with the present invention;

**FIG. 3A** is a general block diagram of a first embodiment of a microprocessor in accordance with the present invention;

**FIG. 3B** is a general block diagram of a second embodiment of a  
25 microprocessor in accordance with the present invention; and

**FIG. 3C** is a general block diagram of one embodiment of a microprocessor in accordance with the present invention.

DETAILED DESCRIPTION OF THE  
PRESENTLY PREFERRED EMBODIMENTS

Referring to **FIG. 2**, SRAM **20a** and SRAM **20b** are mounted upon  
5 processor card **10** as previously described in connection with **FIG. 1**. In  
accordance with the present invention, pin **22a** and pin **26b** are electrically  
coupled via a conductor **29a** within processor card **10** to concurrently receive a  
first address bit signal. Pin **23a** and pin **25b** are electrically coupled via a  
conductor **29b** within processor card **10** to concurrently receive a second  
10 address bit signal. Pin **25a** and pin **23b** are electrically coupled via a conductor  
**29c** within processor card **10** to concurrently receive a third address bit signal.  
Pin **26a** and pin **22b** are electrically coupled via a conductor **29d** within processor  
card **10** to concurrently receive a fourth address bit signal. The length of the  
conductors **29a-29d** facilitate an effective and efficient operation of SRAM **20a**  
15 and SRAM **20b** over a wide range of operating frequencies of a microprocessor.

Referring to **FIG. 3A**, a microprocessor **30** in accordance with the present  
invention for selecting between two (2) of the four (4) cache configurations  
supported by SRAM **20a** and SRAM **20b** is shown. Microprocessor **30** includes  
main logic units **31** for interpreting and executing operating and application  
20 programs as would occur to one skilled in the art. Microprocessor **30** further  
includes a controller **32** and a multiplexer **33**. Address bus **32a** and address bus  
**32b** provide electrical communication between controller **32** and multiplexer **33**.  
Address bus **32a** and address bus **32b** each have two (2) address lines.  
Multiplexer **33** has an address bus **33a** with a first address line electrically  
25 coupled to pin **22a** (**FIG. 2**) and pin **26b** (**FIG. 2**), and a second address line  
electrically coupled to pin **26a** (**FIG. 2**) and pin **22b** (**FIG. 2**). The following Table  
1 exemplary illustrates an address bit logic utilized by main logic units **31** for  
electrically communicating a selected cache configuration between an 8 Mbyte  
cache and a 16 Mbyte cache to SRAM **20a** and SRAM **20b**.

TABLE 1

ADDRESS BUS	CACHE SIZE	FIRST ADDRESS LINE (MSB)	SECOND ADDRESS LINE (LSB)
32a	8 Mbyte	net2	net2
32b	16 Mbyte	net1	net2

Still referring to **FIG. 3A**, microprocessor **30** further comprises a

5 configuration register **34**. Configuration register **34** provides a control signal to multiplexor **33** via a control bus **34a** in response to a selection signal from main logic units **31** via a data bus **31a**. The selection signal is indicative of a selected cache configuration by main logic units **31** during an initial boot of microprocessor **30**. The control signal is indicative of the address bus that

10 corresponds to the selected cache configuration. Consequently, multiplexor **33** provides the appropriate address signals via address bus **33a** to SRAM **20a** and SRAM **20b** in response to the selection signal. For example, when the selection signal indicates the 16 Mbyte cache has been selected during an initial boot of microprocessor **30**, pin **22a** and pin **26b** concurrently receive address signal

15 net1, and pin **26a** and pin **22b** concurrently receive address signal net2 as indicated by Table 1.

Referring to **FIG. 3B**, a microprocessor **40** in accordance with the present invention for selecting between three (3) of the four (4) cache configurations supported by SRAM **20a** and SRAM **20b** is shown. Microprocessor **40** includes

20 main logic units **41** for interpreting and executing operating and application programs as would occur to one skilled in the art. Microprocessor **40** further includes a controller **42** and a multiplexer **43**. Address bus **42a**, address bus **42b**, and address bus **42c** provide electrical communication between controller

42 and multiplexer 43. Address bus 42a address bus 42b, and address bus 42c each have three (3) address lines. Multiplexer 43 has an address bus 43a with a first address line electrically coupled to pin 22a (FIG. 2) and pin 26b (FIG. 2), a second address line electrically coupled to pin 26a (FIG. 2) and pin 22b (FIG. 2), and a third address line electrically coupled to pin 23a (FIG. 2) and pin 25b (FIG. 2). The following Table 2 exemplary illustrates the address bit logic utilized by main logic units 41 for electrically communicating a selected cache configuration between a 4 Mbyte cache, an 8 Mbyte cache and a 16 Mbyte cache to SRAM 20a and SRAM 20b.

TABLE 2

ADDRESS BUS	CACHE SIZE	FIRST ADDRESS LINE (MSB)	SECOND ADDRESS LINE	THIRD ADDRESS LINE (LSB)
32a	4 Mbyte	net3	net3	net3
32b	8 Mbyte	net2	net2	net3
32c	16 Mbyte	net1	net2	net3

Still referring to FIG. 3B, microprocessor 40 further comprises a configuration register 44. Configuration register 44 provides a control signal to multiplexer 43 via a control bus 44a in response to a selection signal from main logic units 41 via a data bus 41a. The selection signal is indicative of a selected cache configuration by main logic units 41 during an initial boot of microprocessor 40. The control signal is indicative of the address bus that corresponds to the selected cache configuration. Consequently, multiplexer 43 provides the appropriate address signals via address bus 43a to SRAM 20a and SRAM 20b in response to the selection signal. For example, when the selection



signal indicates the 8 Mbyte cache has been selected, pin **22a** and pin **26b** concurrently receive address signal net2, pin **26a** and pin **22b** concurrently receive address signal net2, and pin **23a** and pin **25b** concurrently receive address signal net3 as indicated by Table 2.

Referring to **FIG. 3C**, a microprocessor **50** in accordance with the present invention for selecting between all four (4) cache configurations supported by SRAM **20a** and SRAM **20b** is shown. Microprocessor **50** includes main logic units **51** for interpreting and executing operating and application programs as would occur to one skilled in the art. Microprocessor **50** further includes a controller **52** and a multiplexer **53**. Address bus **52a**, address bus **52b**, address bus **52c**, and address bus **52d** provide electrical communication between controller **52** and multiplexer **53**. Address bus **52a** address bus **52b**, address bus **52c**, and address bus **52d** each have four (4) address lines. Multiplexer **53** has an address bus **53a** with a first address line electrically coupled to pin **22a** (**FIG. 2**) and pin **26b** (**FIG. 2**), a second address line electrically coupled to pin **26a** (**FIG. 2**) and pin **22b** (**FIG. 2**), a third address line electrically coupled to pin **23a** (**FIG. 2**) and pin **25b** (**FIG. 2**), and a fourth address line electrically coupled to pin **23b** (**FIG. 2**) and pin **25a** (**FIG. 2**). The following Table 3 exemplary illustrates the address bit logic utilized by main logic units **51** for electrically communicating a selected cache configuration between a 2 Mbyte cache, a 4 Mbyte cache, an 8 Mbyte cache and a 16 Mbyte cache to SRAM **20a** and SRAM **20b**.

TABLE 3

<i>ADDRESS BUS</i>	<i>CACHE SIZE</i>	<i>FIRST ADDRESS LINE (MSB)</i>	<i>SECOND ADDRESS LINE</i>	<i>THIRD ADDRESS LINE</i>	<i>FOURTH ADDRESS LINE (LSB)</i>
32a	2 Mbyte	net4	net4	net4	net4
32b	4 Mbyte	net3	net3	net3	net4
32c	8 Mbyte	net2	net2	net3	net4
32d	16 Mbyte	net1	net2	net3	net4

Still referring to **FIG. 3C**, microprocessor **50** further comprises a configuration register **54**. Configuration register **54** provides a control signal to multiplexor **53** via a control bus **54a** in response to a selection signal from main logic units **51** via a data bus **51a**. The selection signal is indicative of a selected cache configuration by main logic units **51** during an initial boot of microprocessor **50**. The control signal is indicative of the address bus that corresponds to the selected cache configuration. Consequently, multiplexor **53** provides the appropriate address signals via address bus **53a** to SRAM **20a** and SRAM **20b** in response to the selection signal. For example, when the selection signal indicates the 8 Mbyte cache has been selected, pin **22a** and pin **26b** concurrently receive address signal net2, pin **26a** and pin **22b** concurrently receive address signal net2, pin **23a** and pin **25b** concurrently receive address signal net3, and pin **23b** and pin **25a** concurrently receive address signal net4 as indicated by Table 3.

From the previous description of SRAM **20a** and SRAM **20b** herein in connection with **FIG. 2**, one skilled in the art will know how to make and use electrical couplings between additional synchronous address pins of SRAM **20a** and SRAM **20b** in accordance with the present invention. From the previous description of microprocessors **30**, **40**, and **50** in connection with **FIGS. 3A-3C**, respectively, one skilled in the art will know how to make and use microprocessors in accordance with the present invention for selecting a cache configuration between five or more supported cache configurations.

While the embodiments of the present invention disclosed herein are presently considered to be preferred, various changes and modifications can be made without departing from the spirit and scope of the invention. The scope of the invention is indicated in the appended claims, and all changes that come within the meaning and range of equivalents are intended to be embraced therein. For examples, the pin configuration and size of SRAM **20a** and SRAM **20b** can vary, and/or SRAM **20a** and SRAM **20b** may include asynchronous address pins. Additionally, SRAM **20a** and SRAM **20b** may be misaligned along the respective sides of processor card **10**, and/or mounted on the same side of processor card **10**. Also, other memory devices may be utilized in lieu of SRAM **20a** and SRAM **20b**, e.g. dynamic static random access memories.